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**AMENDMENTS TO THE CLAIMS:**

**Please cancel claim 36 without prejudice or disclaimer.**

1-10 (Canceled)

11. (Currently amended) An array of microelectronic elements comprising:  
a substrate of semiconductor material;  
a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto;  
a pattern of mutually electrically isolated conducting regions disposed within said lower layer of dielectric material, said conducting regions extending to said upper surface of said lower layer;  
an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer; and  
a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer; and  
a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer,  
wherein each conducting region comprises:  
a metal conductor; and  
a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node.

12. (Previously presented) An array as set forth in claim 11, wherein each of said nodes comprises a semiconductor device.

13. (Previously presented) An array as set forth in claim 11, wherein said semiconductor material comprises oriented single crystal grain, monocrystalline semiconductor material, and

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each of said nodes comprises a diode.

14. (Original) An array as set forth in claim 13, wherein said microelectronic elements comprise magnetoresistive memory elements each comprising a said diode and an MTJ structure.

15. (Previously presented) An array as set forth in claim 12, wherein said semiconductor device comprises a field effect transistor.

16. (Previously presented) An array as set forth in claim 15, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer.

17. (Previously presented) An array as set forth in claim 13, wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation.

18. (Previously presented) An array as set forth in claim 11, wherein said electrically conducting material comprises at least one of W, Ti, and Ta.

19-25 (Canceled)

26. (Currently amended) A microelectronic element array comprising:  
a semiconductor substrate;  
a first dielectric layer formed on said substrate;  
a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:  
a metal conductor; and  
a conductive via which is filled with a diffusion barrier material formed on said metal conductor;  
a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer; and

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a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by said conductive via; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and a node in said plurality of nodes.

27. (Previously presented) The array according to claim 26, wherein said plurality of semiconductor nodes comprises a plurality of monocrystalline semiconductor diodes.

28. (Previously presented) The array according to claim 26, wherein each conductive region extends from said substrate to said upper surface of said first dielectric layer.

29. (Previously presented) The array according to claim 26, wherein each conductive region further comprises a word line, said via being formed on said word line.

30. (Previously presented) The array according to claim 27, further comprising:  
a plurality of magnetic tunnel junction (MTJ) elements, each MTJ element in electrical contact with a diode in said plurality of monocrystalline semiconductor diodes.

31. (Previously presented) The array according to claim 30, wherein each said MTJ element and each said diode combine to form a memory element.

32. (Canceled)

33. (Previously presented) The array according to claim 26, wherein said via includes therein at least one of W, Ti, and Ta.

34. (Previously presented) The array according to claim 26, wherein each said conductive

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region further comprises a metal layer in electrical contact with said via, said metal layer being formed of a different material than said via.

35. (Previously presented) The array according to claim 29, wherein said via includes therein a refractory metal and said word line comprises one of copper and aluminum.

36. (Canceled)

37. (Currently amended) The array as set forth in claim 11 36, wherein said bonding promoting layer comprises a glass layer having a softening temperature in a range of 400°C to 500°C.

38. (Currently amended) A microelectronic element array comprising:  
a first dielectric layer formed on a substrate;  
at least one electrically isolated conductive region formed in said first dielectric layer, said at least one conductive region comprising:  
a metal conductor; and  
a conductive via which is filled with a diffusion barrier material formed on said metal conductor;  
a second dielectric layer which is bonded to said first dielectric layer; and  
at least one semiconductor node formed in said second dielectric layer, said at least one semiconductor node being formed on and contacting said at least one conductive region; and  
a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding a lower surface of said second dielectric layer to an upper surface of said first dielectric layer,  
wherein said diffusion barrier material extends between said metal conductor and said at least one semiconductor node and electrically connects said metal conductor to said at least one semiconductor node.

39. (Previously presented) The array as set forth in claim 11, wherein said via comprises

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an area which is less than an area of said metal conductor.

40. (Previously presented) The array as set forth in claim 11, wherein said diffusion barrier material comprises one of TiN, TaN and a TaSiN ternary alloy.

41. (Previously presented) The array as set forth in claim 11, wherein said node which is electrically connected to said metal conductor is aligned with said via and said metal conductor.

42. (Previously presented) The array as set forth in claim 11, wherein said node comprises a semiconductor diode.

43. (Previously presented) The array as set forth in claim 11, wherein said metal conductor and said semiconductor material in said node are separated by said diffusion barrier material.